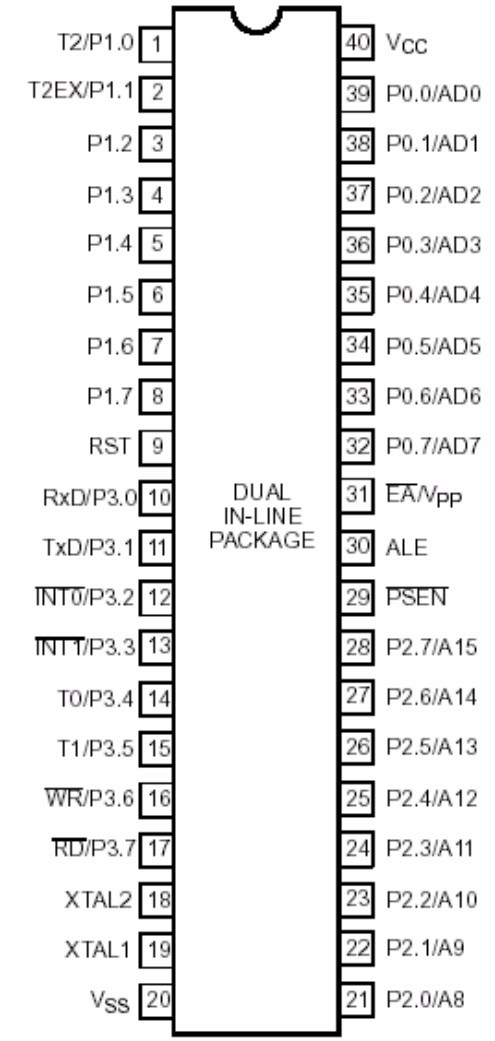
Micros 1

Hardware Interfacing

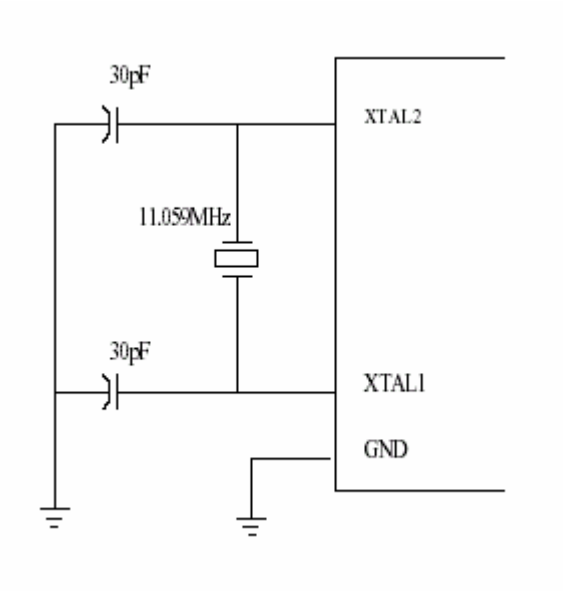
8051 Pin-out

- Power - Vcc, Vss
- Reset - RST
- Crystal - XTAL[1,2]
- External device interfacing
  - EA, ALE, PSEN, WR, RD
- I/O Port
  - P0[7;0], P1[7:0], P2[7:0], P3
- P3 is shared with control lines
  - Serial I/O RxD, TxD,
  - external interrupts INT0, INT1
  - Counter control T0, T1
- P0 and P2 are multiplexed with Address and Data bus



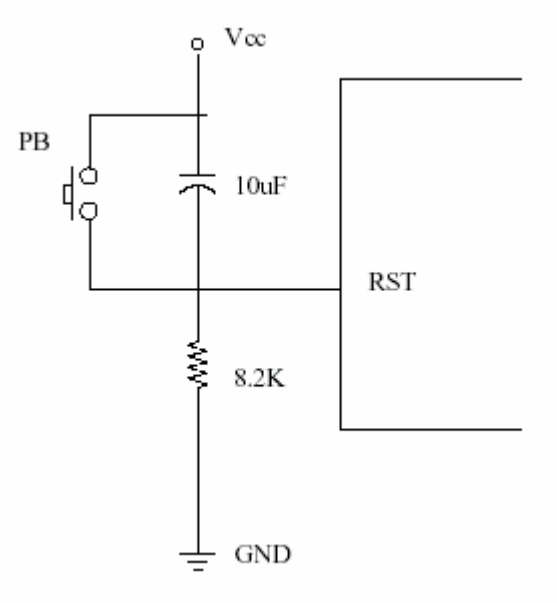
8051 Clock

- 8051 has an on-chip oscillator
- It needs an external crystal
- Standard connection as shown
- Crystal decides the operating frequency of the 8051



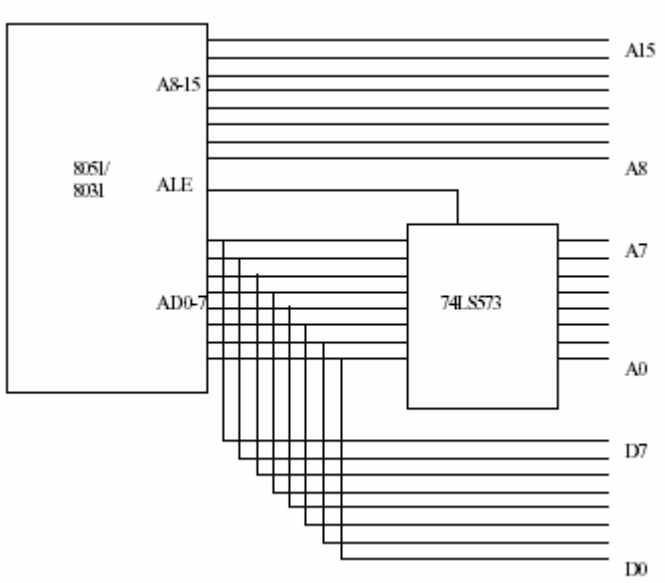
8051 Reset

- RESET is an active High input
- When RESET is set to High, 8051 goes back to the poweron state
- Power-On Reset
  - Push PB and active High is applied on RST input.
  - Release PB, Capacitor discharges and RST goes low.
- RST must stay high for a min of 2 machine cycles



8051 – Address Bus De-mutiplexing

- ALE – Address Latch Enable
- 8051 drives it high when address is available on AD[7,0]
- ALE is used as the “Enable” signal for an external latch (74LS573 or 373)
- P0 and P2 unavailable



8051 External Code Memory Access

- 8051 devices can have either on-chip or external code ROM
- Input pin EA decides which is used and PSEN is used to enable it.
- EA is an active low input to 8051
  - EA connected to GND (Low) means 8051 uses external memory for code
  - EA connected to Vcc (High) means 8051 uses on-chip ROM for code memory
- PSEN – Program Store Enable, active low
  - Connect this to the OE (output enable) of external ROM device

Microprocessor Interfacing - Basics

- Any CPU (8051) has
  - Address bus A[15:0]
  - Data bus D[7:0]
  - Control lines : ALE, PSEN, RD, WR
- A Single Processor μP based system has one CPU and many devices **interfaced** to it
- Only one Address bus and one data bus in a Single Processor system
  - ABUS and DBUS are common for all interfaced devices and the CPU

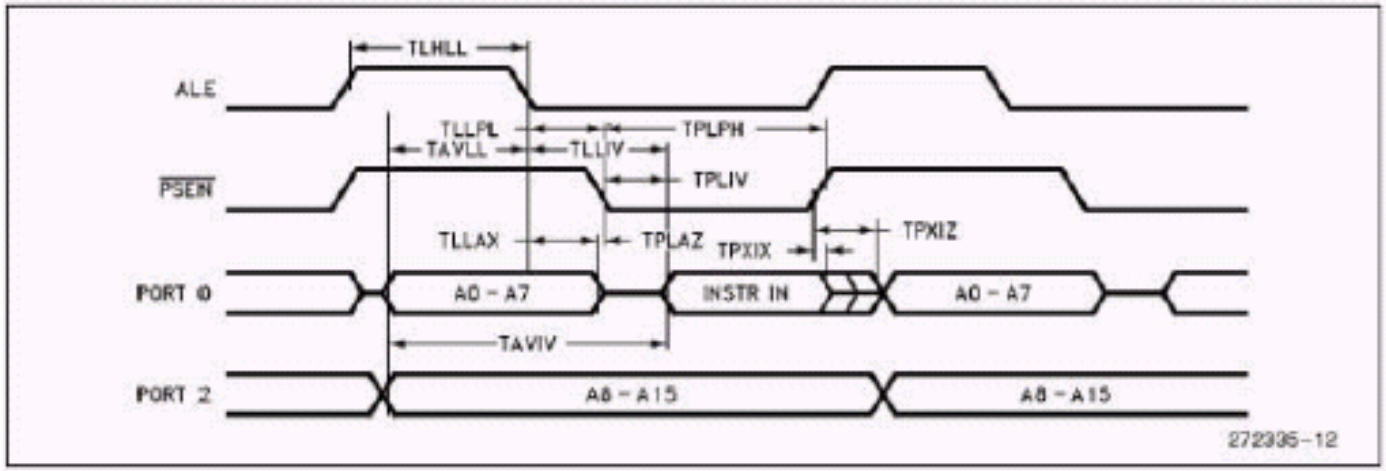
Microprocessor Interfacing (contd.)

- All Microprocessor compatible devices have enable lines (CE - Chip Enable or CS – Chip Select)
  - A **function** of the address bus ***f(A[15:0])*** is connected to the CE of every device interfaced
  - This function is **unique** for every interfaced device
- The CPU accesses each interfaced device by way of this unique function
  - This function is commonly referred to as the **address of the device**

Microprocessor Interfacing (contd.)

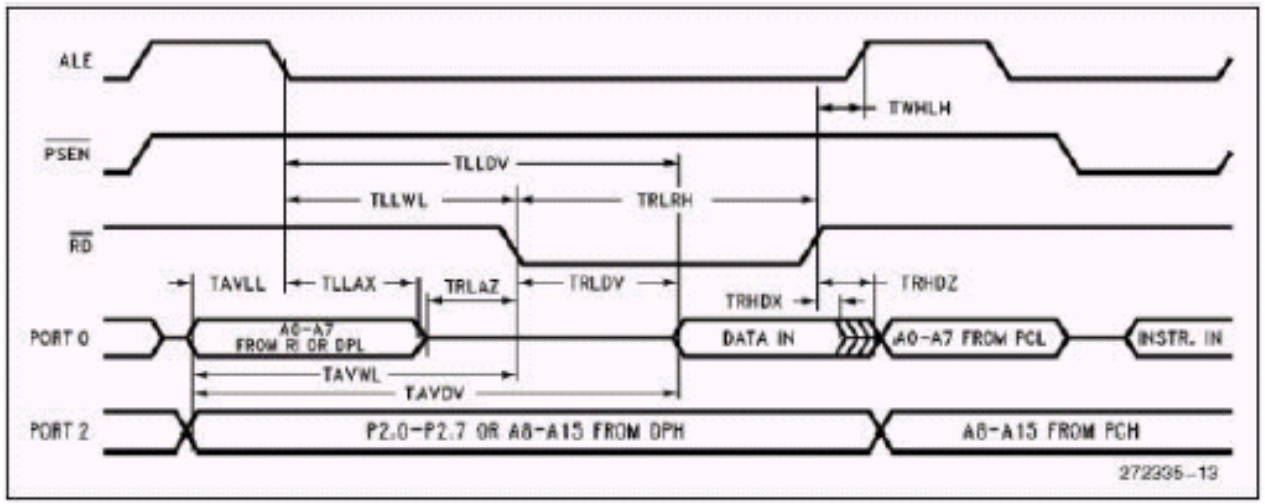
- Interfaced devices either READ or WRITE or do BOTH on the DBUS.
  - Only one device has ***"exclusive access"***
  - Achieved by using Tri-State buses
- Devices that WRITE to DBUS have CE and RD/OE only
  - Read Cycle: Assert CE and then assert RD/OE
- Devices that READ and WRITE to DBUS have CE, RD/OE and WR
  - Write Cycle: Assert CE and then assert WR

8051 Code Memory Read Cycle



- 12MHZ part 87C51BH
- TLLIV – ALE low to valid Instr → 234ns max
- TPLIV – PSEN low to valid Instr → 145ns max
- TAVIV – Addr valid to valid Instr → 312ns max
- TPLPH – PSEN pulse width → 205ns min

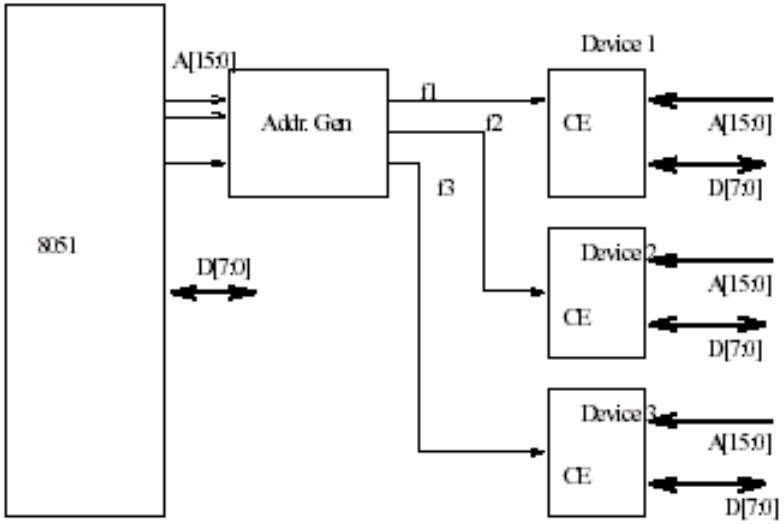
8051 Data Memory Read Cycle



- TRLDV – RD Low to valid Data → 252ns max
- TAVDV – Addr valid to valid Data → 585ns max
- TLLDV – ALE low to valid Data → 517ns max
- TRLRH – RD pulse width → 400ns min

8051 – Address Generation

- Address Generator is a piece of hardware that produces unique addresses to each interfaced device
- Example
  - F1 = A15 . $\overline{A14}$
  - F2 = A15 . $\overline{A14}$
  - F3 = $\overline{A15}$. $\overline{A14}$



What is needed ?

- Need to know the following for **all** the devices before address generator can be designed
  - Base address of each device
    - Where it starts in the address map
  - Size of the device
    - How much of the address space it uses up

Example –1 : 2K Memory at 0x0000

- Pins : address – A10 to A0, Data – D7 to D0, $\overline{RD}$, $\overline{WR}$, $\overline{CE}$
- Base address = 0x0000
- Size = 2k (2 *1024 = 2048 bytes = 0x0800)
- Address Map occupancy
  - 0x0000 to 0x07FF that is,
  - 0000 - 0000 - 0000 - 0000 binary to
  - 0000 - 0111 - 1111 - 1111 binary
- 11 lowest address bits A10 to A0 have to be connected to the address pins on the memory

Example –1 : (contd.)

- Unused address bits are
  - A15 to A11
- Base address is 0x0000
- CE has to be generated if all the unused address bits are logic-0
  - CE is active low
- $\overline{CE}$ = A15 + A14 + A13 + A12 + A11
- Then connect $\overline{RD}$ and $\overline{WR}$

A15	A14	A13	A12	A11	$\overline{CE}$
0	0	0	0	0	0
X	X	X	X	1	1
X	X	X	1	X	1
X	X	1	X	X	1
X	1	X	X	X	1
1	X	X	X	X	1

Example 2: Same Memory at 0x4000

- Base address is 0x4000
  - 0100 0000 0000 0000
- Size is 2K
- Unused address bits
  - A15 to A11
- CE has to be generated as per the truth-table
- Expression is:

$$\overline{CE} = \overline{A15}.A14.\overline{A13}.\overline{A12}.\overline{A11}$$

A15	A14	A13	A12	A11	$\overline{CE}$
X	0	X	X	X	1
0	1	0	0	0	0
X	1	X	X	0	1
X	1	X	X	1	1
X	1	X	0	X	1
X	1	X	1	X	1
and	so	on			

Complete vs. Partial Address Decoding

- Complete address decoding:
  - Use all unused address bits to generate CE
- Partial addressing decoding
  - Use a sub-set of the unused address bits
  - Used to reduce the address generator complexity
  - Produces address mirrors (same device at multiple addresses)
- Example
  - 2K memory at 0x0000, we used A15 to A11
  - Instead just connect A11 to $\overline{CE}$
  - Same 2K memory device will then be mirrored for all values of A15 to A12
    - 0x0000, 0x1000, 0x2000, 0x3000, …. , 0xF000
  - Address generator became very simple, but we lost a lot of address space

74138 Decoder for Address Generation

- 3 to 8 decoder, available in a single DIP package.
- Takes 3 address lines and generates complete addressing among those
- Example
  - Connect A15, A14, A13 to the decoder inputs
  - Decoder outputs give base addresses for
    - 0x0000, 0x2000, 0x4000, 0x6000,0x8000, 0xA000, 0xC000, 0xE000
- For more complicated address decoding:
  - Play tricks with 74138 enable connections.
  - Use programmable devices like PALs, PLDs or FPGAs

External Pure Code Memory

- Could be RAM or ROM
- Address generation as per standard procedure
- Connect $\overline{\text{PSEN}}$ to the $\overline{\text{OE}}$ of the memory device
  - $\overline{\text{RD}}$ and $\overline{\text{WR}}$ are ignored
- Connect Data bits D7-D0 of the memory and the 8051

External Code + Data Memory

- Address generation as per standard procedure
- Logically AND $\overline{PSEN}$ and $\overline{RD}$ and then connect to the $\overline{OE}$ of the memory
- Connect $\overline{WR}$ from the 8051 to WR of the memory
- Connect Data bits D7-D0 of the memory and the 8051

External I/O Devices

- Same procedure as for interfacing memory
- Only difference is that these devices have smaller sizes and use smaller portions of the address space
- Example:
  - 8 LEDS connected to an 8-bit latch. The latch is address mapped to 0xF000. Size is 1byte
  - 8255 I/O device memory mapped at 0xD000. Size is 4 bytes

Electrical Considerations

ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

PARAMETER	RATING	UNIT
Operating temperature under bias	0 to +70 or –40 to +85	°C
Storage temperature range	–65 to +150	°C
Voltage on $\overline{EA}/V_{PP}$ pin to V_{SS}	0 to +13.0	V
Voltage on any other pin to V_{SS}	–0.5 to +6.5	V
Maximum I_{OL} per I/O pin	15	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.5	W

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

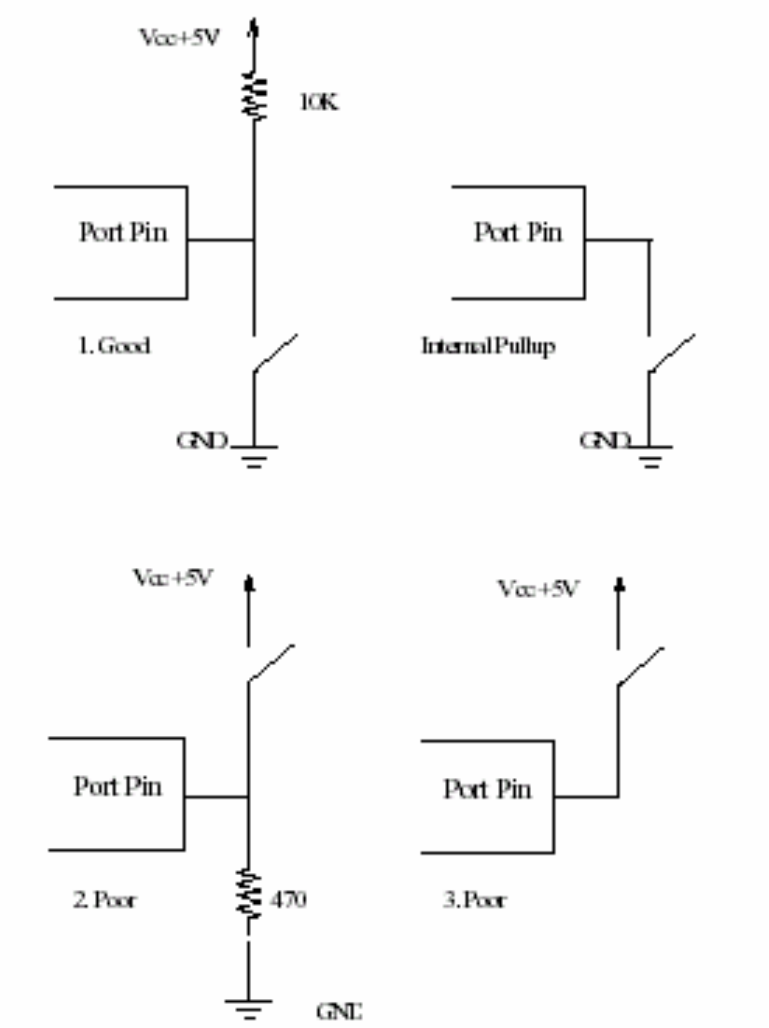
Electrical Characteristics (Contd.)

DC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C or –40°C to +85°C, V_{CC} = 2.7V to 5.5V, V_{SS} = 0V (16MHz devices)

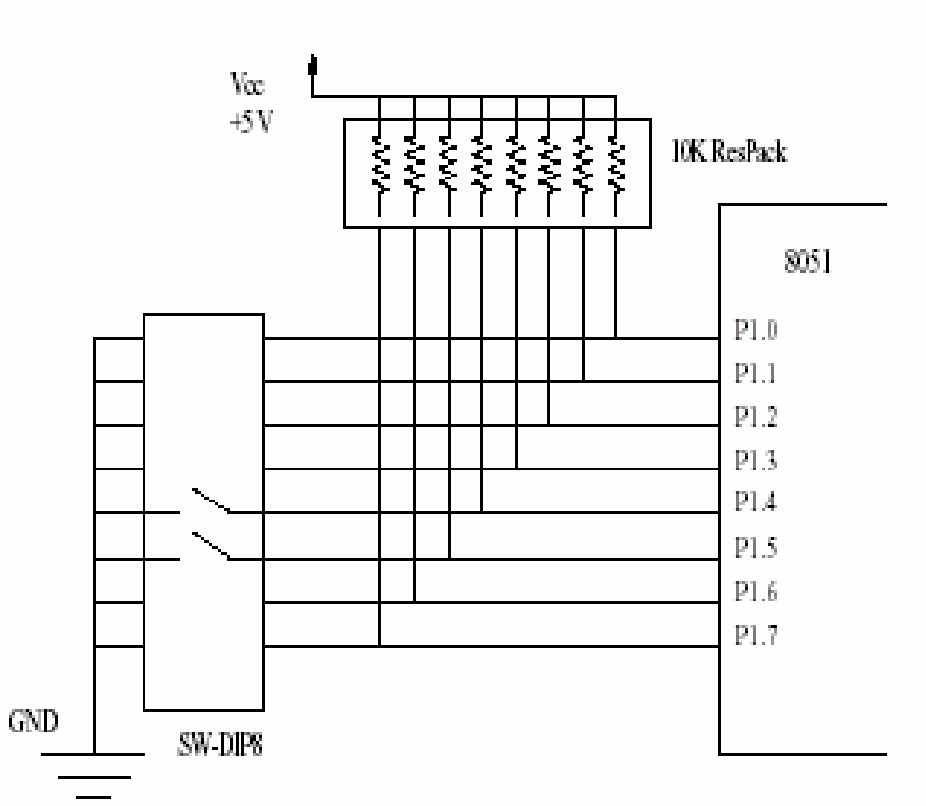
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
V_{IL}	Input low voltage	4.0V < V_{CC} < 5.5V	–0.5		$0.2V_{CC}$–0.1	V
		2.7V<V_{CC}< 4.0V	–0.5		0.7	V
V_{IH}	Input high voltage (ports 0, 1, 2, 3, $\overline{EA}$)		$0.2V_{CC}$+0.9		V_{CC}+0.5	V
V_{IH1}	Input high voltage, XTAL1, RST		$0.7V_{CC}$		V_{CC}+0.5	V
V_{OL}	Output low voltage, ports 1, 2, [8]	V_{CC} = 2.7V I_{OL} = 1.6mA[2]			0.4	V
V_{OL1}	Output low voltage, port 0, ALE, $\overline{PSEN}$[8, 7]	V_{CC} = 2.7V I_{OL} = 3.2mA[2]			0.4	V
V_{OH}	Output high voltage, ports 1, 2, 3 [3]	V_{CC} = 2.7V I_{OH} = –20µA	V_{CC} – 0.7			V
		V_{CC} = 4.5V I_{OH} = –30µA	V_{CC} – 0.7			V
V_{OH1}	Output high voltage (port 0 in external bus mode), ALE[9], $\overline{PSEN}$[3]	V_{CC} = 2.7V I_{OH} = –3.2mA	V_{CC} – 0.7			V
I_{IL}	Logical 0 input current, ports 1, 2, 3	V_{IN} = 0.4V	–1		–50	µA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3[6]	V_{IN} = 2.0V See note 4			–650	µA
I_{LI}	Input leakage current, port 0	0.45 < V_{IN} < V_{CC} – 0.3			±10	µA

8051 - Switch On IO Ports



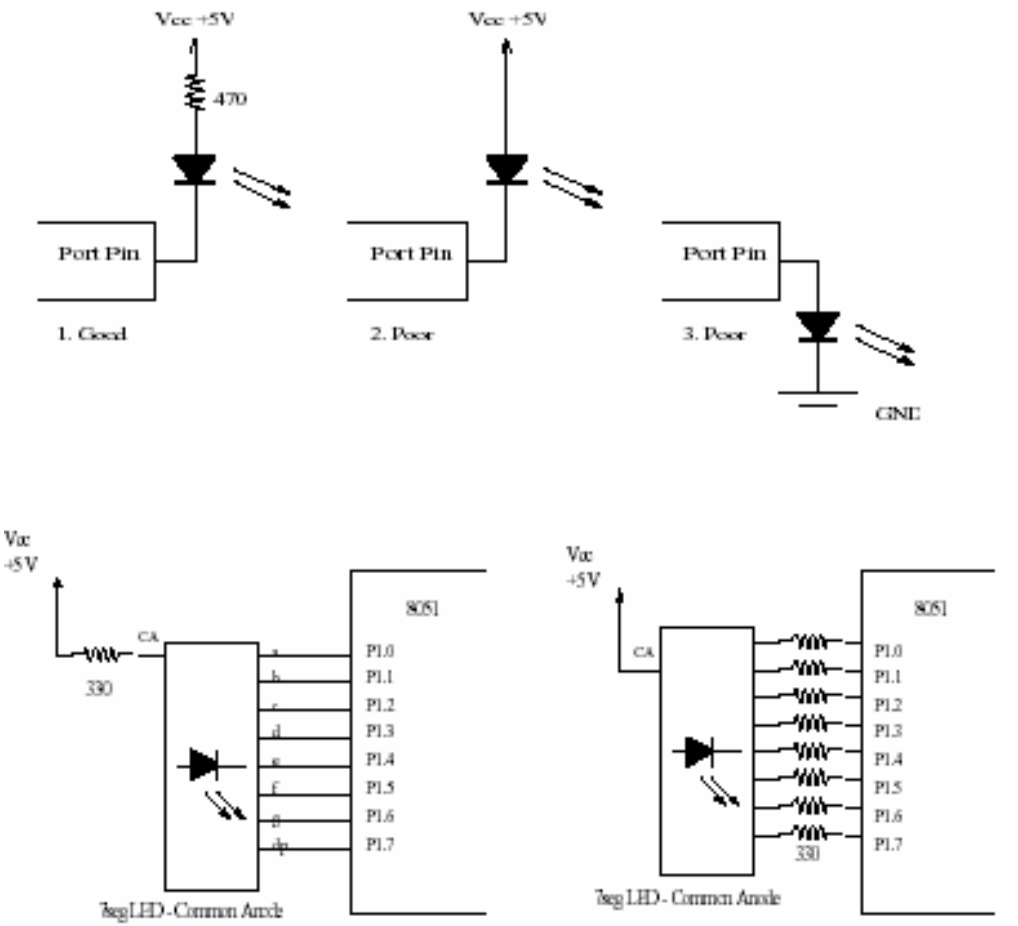
- Case-1:
  - Gives a logic 0 on switch close
  - Current is 0.5ma on switch close
- Case-2:
  - Gives a logic 1 on switch close
  - High current on switch close
- Case-3:
  - Can damage port if 0 is output

DIP Switches on IO port



- DIP switches usually have 8 switches
- Use the case-1 from previous page
- Can use a Resistor Pack, instead of discrete resistors

LED on IO Port



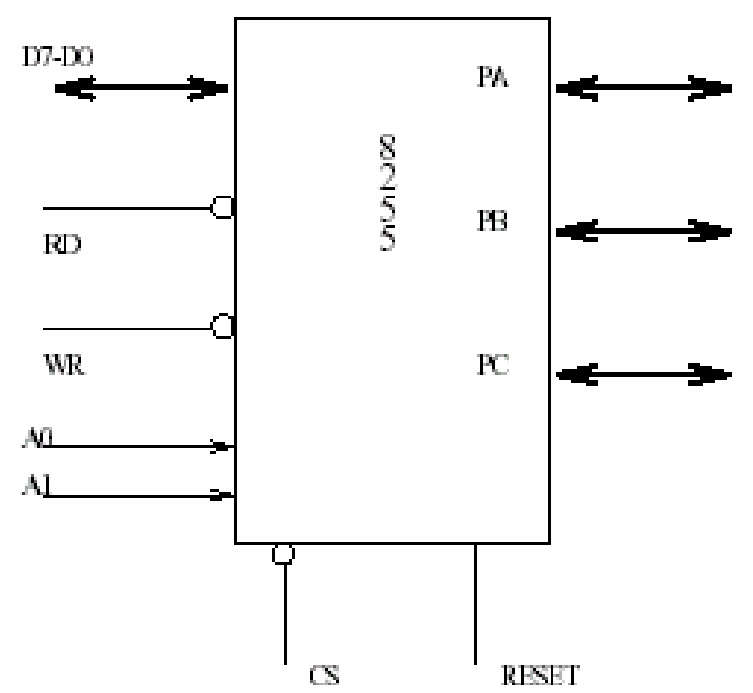
- Try to use current sinking
- Case-1
  - LED is ON for an output of zero
  - Most LEDs drop 1.7 to 2.5 volts and need about 10ma
  - Current is (5-2)/470
- Case-2
  - Too much current
  - Failure of Port or LED
- Case-3
  - Not enough drive (1ma)
  - LED too dim
- Seven Segment LEDs
  - Common Anode/ Cathode
  - CA preferred
  - Case-1 may have LEDs of different brightness

8051 Interfacing with the 8255

- 8255 - Widely used I/O chip
  - 40 pins
  - Provides 3 eight bit ports PA, PB and PC
  - Port PC can be used as two 4 bit ports PCL and PCU
  - Ports have handshaking ability
  - Two address lines A0, A1 and a Chip select CS
    - Address space of 4 bytes
    - 00b selects Port A
    - 01b selects Port B
    - 10b selects Port C
    - 11b selects an internal control register
      - Read only.

8255 Functional Diagram

- CS is used to interface with 8051
- If CS is generated from lets say Address lines A15:A12 as follows,
  A15:A12 = 1000
- Base address of 8255 is
  - 1000 xxxx xxxx xx00b
  - 8000H
- Address of the registers
  - PA = 8000H
  - PB = 8001H
  - PC = 8002H
  - CR = 8003H



8255 Operating Modes

- Mode 0 : Simple I/O
  - Any of A, B, CL and CU can be programmed as input or output
- Mode 1: I/O with Handshake
  - A and B can be used for I/O
  - C provides the handshake signals
- Mode 2: Bi-directional with handshake
  - A is bi-directional with C providing handshake signals
  - B is simple I/O (mode-0) or handshake I/O (mode-1)
- BSR (Bit Set Reset) Mode
  - C alone is available for bit mode access
    - Allows single bit manipulation for control applications.

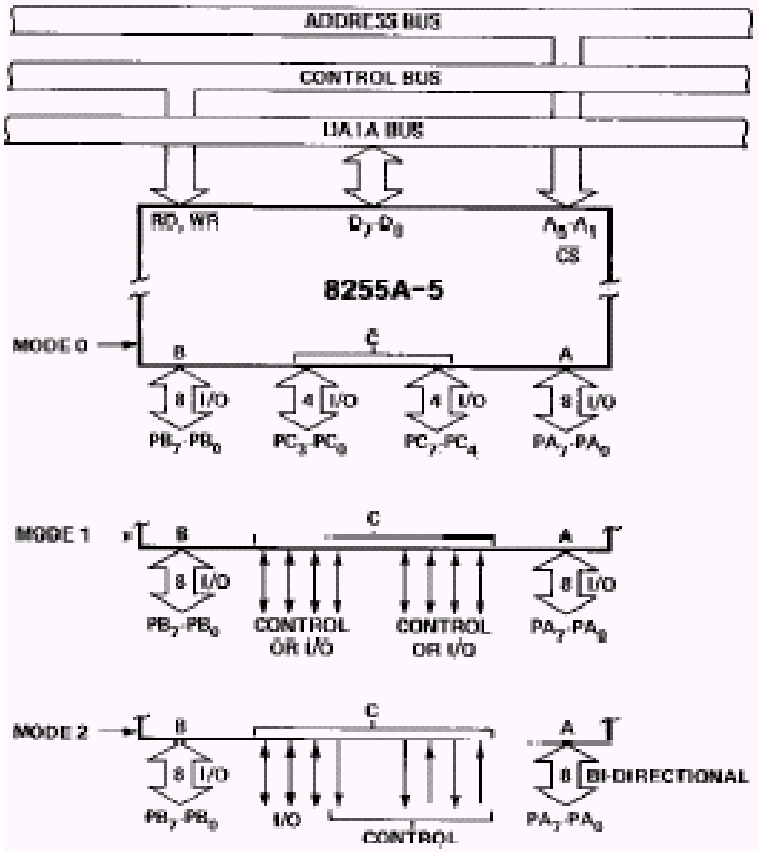
8255 Mode Definition Summary

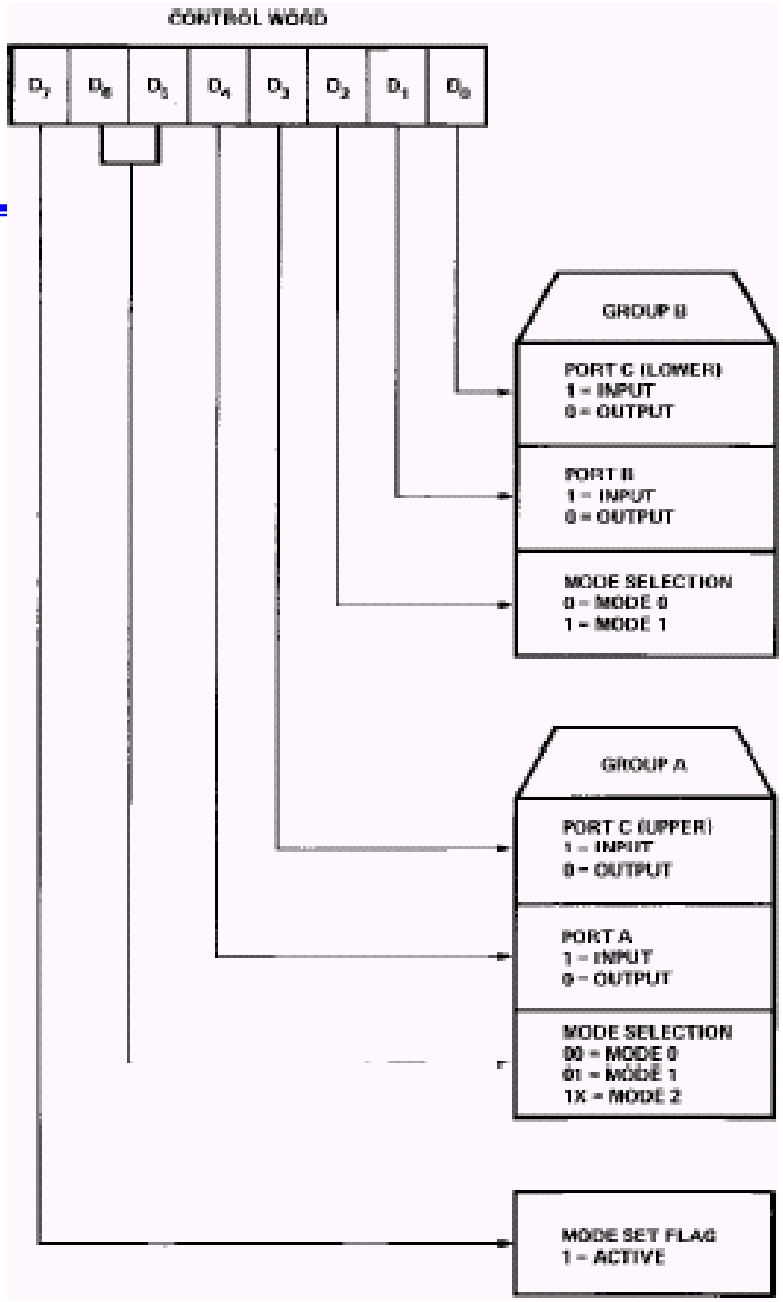
	MODE 0		MODE 1		MODE 2
	IN	OUT	IN	OUT	GROUP A ONLY
PA_0	IN	OUT	IN	OUT	⟷
PA_1	IN	OUT	IN	OUT	⟷
PA_2	IN	OUT	IN	OUT	⟷
PA_3	IN	OUT	IN	OUT	⟷
PA_4	IN	OUT	IN	OUT	⟷
PA_5	IN	OUT	IN	OUT	⟷
PA_6	IN	OUT	IN	OUT	⟷
PA_7	IN	OUT	IN	OUT	⟷
PB_0	IN	OUT	IN	OUT	—
PB_1	IN	OUT	IN	OUT	—
PB_2	IN	OUT	IN	OUT	—
PB_3	IN	OUT	IN	OUT	—
PB_4	IN	OUT	IN	OUT	—
PB_5	IN	OUT	IN	OUT	—
PB_6	IN	OUT	IN	OUT	—
PB_7	IN	OUT	IN	OUT	—
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O
PC_1	IN	OUT	IBF_B	$\overline{OBF}_B$	I/O
PC_2	IN	OUT	$\overline{STB}_B$	$\overline{ACK}_B$	I/O
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$
PC_4	IN	OUT	$\overline{STB}_A$	I/O	$\overline{STB}_A$
PC_5	IN	OUT	IBF_A	I/O	IBF_A
PC_6	IN	OUT	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$
PC_7	IN	OUT	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$

8255 Configuration

- Configured by writing a **control-word** in CR register
- CR definition
  - D7 : 1→I/O mode, 0 → BSR
  - D6,D5 : Mode selection for A and CU
    - 00 → Mode0, 01 → Mode1, 1x → Mode2
  - D4 : Port A control
    - 1 → A input, 0 → A output
  - D3 : Port CU control
    - 1 → CU input, 0 → CU output
  - D2 : Port B Mode selection
    - 0 → B is in mode 0, 1 → B is in mode 1
  - D1 : Port B control
    - 1 → B input, 0 → B output
  - D0 : Port CL control
    - 1 → CL input, 0 → CL output
- Refer to 8255 datasheet for additional options

8255 Control Word





8255 Usage: Simple Example

- 8255 memory mapped to 8051 at address 8000H base
  - PA = 8000H, PB = 8001H, PC = 8002H, CR = 8003H
- Control word for all ports as outputs in mode0
  - CR : 1000 0000b = 80H
- Code segment

```
test:   mov   A, #80H          ; control word
        mov   DPTR, #8003H     ; address of CR
        movx  @DPTR, A         ; write control word
        mov   A, #55h          ; will try to write 55 and AA alternatively
repeat: mov   DPTR, #8000H     ; address of PA
        movx  @DPTR, A         ; write 55H to PA
        inc   DPTR             ; now DPTR points to PB
        movx  @DPTR, A         ; write 55H to PB
        inc   DPTR             ; now DPTR points to PC
        movx  @DPTR, A         ; write 55H to PC
        cpl   A                ; toggle A (55→AA, AA→55)
        acall MY_DELAY         ; small delay subroutine
        sjmp  repeat           ; for (1)
```

BSR Mode

- If used in BSR mode, then the bits of port C can be set or reset individually.